What is claimed is:

1. A floating gate having improved coupling ratio, comprising:

a semiconductor substrate;

a tunneling dielectric layer formed on the semiconductor substrate;

a conductive layer, formed on the tunneling dielectric layer; and

a plurality of conductive spacers, formed on the sidewalls of the conductive layer, and the tops of the conductive spacers level with the surface of the conductive layer, with the conductive spacers and the conductive layer forming the floating gate.

2. The floating gate as claimed in claim 1, further comprising two neighboring shallow trench isolation structures, and the tunneling dielectric layer located between the two shallow trench isolation structures.

3. The floating gate as claimed in claim 1, wherein the conductive layer is doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide.

4. The floating gate as claimed in claim 1, wherein the conductive spacers are doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide.

5. The floating gate as claimed in claim 1, wherein the tunneling dielectric layer is oxide or oxynitride.

6. The floating gate as claimed in claim 1, wherein the insulation layer is nitride.

7. A floating gate having improved coupling ratio, comprising:

a semiconductor substrate;

a tunneling dielectric layer formed on the semiconductor substrate;

a conductive layer, formed on the tunneling dielectric layer;

a pair of shallow trench isolation formed oppositely adjacent to the conductive layer, wherein the shallow trench isolation is lower than the top surface of the conducting layer; and

a plurality of conductive spacers, formed on the sidewalls of the conductive layer and overlying the shallow trench isolation, and the tops of the conductive spacers level with the surface of the conductive layer, with the conductive spacers and the conductive layer forming the floating gate.

8. The floating gate as claimed in claim 7, wherein the conductive layer is doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide.

9. The floating gate as claimed in claim 7, wherein the conductive spacers are doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide.

10. The floating gate as claimed in claim 7, wherein the tunneling dielectric layer is oxide or oxynitride.

11. The floating gate as claimed in claim 7, wherein the shallow trench isolation is an oxide layer.